UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,309	12/15/2001	Gary Smith	111215REJ.US	2338

30233 7590 02/24/2005

TROPIAN INC.
20813 STEVENS CREEK BLVD.
CUPERTINO, CA 95014

EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,309	SMITH, GARY	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the following informalities:

As to claim 2, in line 12 "is" should be removed before the word "unaffected" .

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, and further in view of Horner et al (US Patent 5,357,544) and Stevenson (US Patent 6,674,812).

As to claims 1 and 3, the admitted prior art teaches a digital RF down converter that comprises of the first frequency down conversion circuit using the local oscillator 110 for down converting the in-phase and quadrature signal components to a first intermediate frequency and the sigma delta ADCs 114 and 116 for generating in-phase and quadrature single bit streams (Fig. 1; Pg. 1, Par. 7; Pg. 2, Par. 8). The admitted prior art is silent about processing the I and Q single digital bit streams through a set of simple logic to produce a digital representation of down converted in-phase and

quadrature components and recombining the digital I and q components with a reconstruction filter in a manner to be substantially free of image artifacts. Horner et al teach a receiving system that mixes the digitized IF signal at the mixer 26 with the reference signal outputted from the reference signal generator unit 24 and finally is low pass filtered at the low pass filter 30 in order for the signal to be recovered (Fig. 2; Col. 3, Lines 51-57; Col. 4, Lines 44 and 45, and Lines 64-67). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Horner et al with the admitted prior art in order to obtain the base-band signal. Stevenson, in the same field of endeavor, teaches a mixer that is constructed by using XOR or XNOR logic according to a clock and summed with a NAND logic (Fig. 1-3; Col. 12, Lines 50-55). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Horner et al and the admitted prior art in order to accomplish image rejection (Fig. 1-3; Col. 12, Lines 50-55).

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Horner et al, and Stevenson, further in view of Jaffe (US Pub. 2004/0223086), and Baltus et al (US Patent 5,808,509).

As to claims 2 and 4, the admitted prior art and Horner et al teach all the subject matters claimed above, except for the reference signal being an over sampled digital word of four bits in length from a source digital oscillator, mixing the reference signal with the serial bit stream according to a clock to achieve at least 16 levels of accuracy, recombining the in phase and quadrature components of the signal in order to obtain a digitally combined signal, and binary weighting the combined reconstructed signal.

Horner et al, teaches the reference signal generator unit 24 that is a periodic over sampled digital word generated from a 128 point cosine wave stored in the cosine table 28 by taking eight entries spaced sixteen points apart (Fig. 2; Col. 4, Lines 55-65). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teaching of Horner et al in order to achieve the desired resolution (Col. 4, Lines 60-64). Jaffe, in the same field of endeavor, teaches the SINE/COS Look up Table 244 being fed by an NCO (Numerically Controlled Oscillator) 242 (Fig. 2; Pg. 3, Par. 26). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Jaffe with the admitted prior art and Horner et al in order to construct a SINE/COS LUT. Jaffe is silent about recombining the in phase and quadrature components of the signal in order to apply binary weighting to the combined signal. Stevenson, in the same field of endeavor, teaches a mixer that is constructed by using XOR or XNOR logic according to a clock and summed with a NAND logic (Fig. 1-3; Col. 12, Lines 50-55). Baltus et al, in the same field of endeavor, teach applying binary weights to the filtered down converted signal and producing Intermediate Frequency signals IF1-IF4 (Fig. 3; Col. 3, Lines 35-43). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Baltus et al with the admitted prior art, Horner et al, Stevenson, and Jaffe in order to use an interpolation network for forming the signals IF1-IF4 (Col. 3, Lines 36 and 37).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Horner et al, and Stevenson as applied to claim 1, further in view of Baltus et al.

As to claim 5, the admitted prior art, Horner et al, and Stevenson teach all the subject matters claimed above, except for the binary weighting employing weighting resistances coupled to the input of the digital reconstruction filter to produce a down coverted signal which is unaffected by the resistor tolerance. Baltus et al, in the same field of endeavor, teach applying binary weights to the filtered down converted signal and producing Intermediate Frequency signals IF1-IF4 (Fig. 3; Col. 3, Lines 35-43). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Baltus et al with the admitted prior art, Horner et al, and Stevenson in order to use an interpolation network for forming the signals IF1-IF4 (Col. 3, Lines 36 and 37).

Claim 6 is rejected under 35 U.S.C. 103 as being unpatentable over the admitted prior art, and further in view of Horner et al and Stevenson.

As to claim 6, the admitted prior art teaches a digital RF down converter that comprises of the first frequency down conversion circuit using the local oscillator 110 for down converting the in-phase and quadrature signal components to a first intermediate frequency and the sigma delta ADCs 114 and 116 for generating in-phase and quadrature single bit streams (Fig. 1; Pg. 1, Par. 7; Pg. 2, Par. 8). The admitted prior art is silent about over sampling the analog signal to obtain an oversampled digital signal, producing a periodic over sampled digital reference signal, and logically combining the digital signal with the digital reference signal to produce and image-canceled digital base-band signal. Horner et al, in the same field of endeavor, teach a receiving system that performs down conversion on the received RF (i.e. Radio Frequency) signal at IF DOWNCOVERTER/FM DISCRIMNATOR 16 and over samples the down converted

signal at the ADC 18 (Fig. 2; Col. 3, Lines 59-66), produces a periodic over sampled digital reference signal 24 (Col. 4, Lines 53-59) and mixes the reference signal with the output of the ADC 18. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Horner et al with the admitted prior art in order to produce base-band I and Q signals. Stevenson, in the same field of endeavor, teaches a mixer/combiner that is constructed by using XOR or XNOR logic according to a clock and summed with a NAND logic (Fig. 1-3; Col. 12, Lines 50-55). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Horner et al and the admitted prior art in order to accomplish image rejection (Fig. 1-3; Col. 12, Lines 50-55).

As to claim 7, the admitted prior art discloses converting the base band digital signal into an analog base band signal by applying the Nyquest 10 bit DACs 128 and 130 (Fig. 1; Pg. 2, Par. 8). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of the admitted prior art with Horner et al and Stevenson in order to recover the signal as analog I and Q components at base-band (Fig. 1; Pg. 2, Par. 8).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, and further in view of Horner et al, Jaffe, Stevenson, and Baltus et al.

As to claim 8, the admitted prior art teaches a digital RF down converter that comprises of the first frequency down conversion circuit using the local oscillator 110 for down converting the in-phase and quadrature signal components to a first intermediate frequency and the sigma delta ADCs 114 and 116 for generating in-phase and

quadrature single bit streams (Fig. 1; Pg. 1, Par. 7; Pg. 2, Par. 8). The admitted prior art is silent about a second digital in-phase and quadrature phase local oscillator, mixing circuitry for mixing respective single serial in-phase and quadrature digital bit streams through a set of logic gates to produce a digital representation of down converted I and Q components, weighting resistances in series with the outputs of the logic gates for combining the digital representation of the down converted I and Q components, and reconstruction filters to recover the I and Q base-band signals. Horner et al, in the same field of endeavor, teach a receiving system that has the Cosine LUT 28 which is inputted to the reference signal generator 24, mixing circuitry for mixing the reference signal with the output of the ADC 18. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Horner et al with the admitted prior art in order to obtain the down converted base band I and Q signal. Horner et al is silent about the mixing circuitry being constructed from a set of logic elements. Stevenson, in the same field of endeavor, teaches a mixer/combiner that is constructed by using XOR or XNOR logic according to a clock and summed with a NAND logic (Fig. 1-3; Col. 12, Lines 50-55). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Stevenson with Horner et al and the admitted prior art in order to accomplish image rejection (Fig. 1-3; Col. 12, Lines 50-55). Horner et al is silent about the second local oscillator to generate the reference signal. Jaffe, in the same field of endeavor, teaches the SINE/COS Look up Table 244 being fed to by an NCO (Numerically Controlled Oscillator) 242 (Fig. 2; Pg. 3, Par. 26). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Jaffe with

Horner et al and the admitted prior art in order to construct the Sine/Cos LUT. Baltus et al, in the same field of endeavor, teach applying weighting resistances in series with the outputs of the digital mixers 20 to the filtered down converted signal and producing Intermediate Frequency (i.e. IF) signals IF1-IF4 (Fig. 3; Col. 3, Lines 35-43). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Baltus et al with Jaffe, Horner et al, and the admitted prior art in order to use an interpolation network for forming the signals IF1-IF4 (Col. 3, Lines 36 and 37). It is well known in the art to use low pass filters in to recover a signal in order to reject the undesirable hormonics.

Allowable Subject Matter

Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 9 and 10, the prior art of record fails to teach the limitations cited in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Khlat et al (US Patent 6,678,340), Reed (US Patent 5,731,781), Marchok et al (5,790,514), Termerinac et al (US Patent 5,881,107).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is (571) 272-6037. The examiner can normally be reached on Monday through Friday 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M. Gh

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER

Freshteh Aghdam

February 14, 2005

***